Amendments to the Claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. (Currently Amended) A film bulk acoustic resonator, comprising:

a semiconductor substrate;

a first resistance layer formed on a surface of the semiconductor substrate, the first resistance layer having a recess;

a membrane layer formed on ~~an upper portion of~~ the first resistance layer [[and]] over the recess, thereby forming in the recess an air gap region of the acoustic resonator; ~~between the membrane layer and the semiconductor substrate at the recess;~~

a first electrode formed on ~~an upper portion of~~ the membrane layer;

a piezoelectric layer formed on ~~the upper portion of~~ the membrane layer and an exposed ~~on an upper~~ portion of the first electrode; and

a second electrode formed on ~~an upper portion of~~ the piezoelectric layer.

2. (Currently Amended) The film bulk acoustic resonator as claimed in claim 1, wherein the semiconductor substrate ~~is controlled to have~~ has a predetermined thickness.

3. (Currently Amended) The film bulk acoustic resonator as claimed in claim 1, further comprising a second resistance layer formed on the first resistance layer. ~~having a predetermined thickness in the recess.~~

4. (Currently Amended) The film bulk acoustic resonator as claimed in claim 3, wherein the second resistance layer has a predetermined thickness in the recess. ~~is on the upper portion of the resistance layer, between the resistance layer and the membrane layer.~~

5. (Currently Amended) The film bulk acoustic resonator as claimed in claim 1, wherein the first resistance layer has a predetermined thickness in the recess.

6. (Original) A method for manufacturing a film bulk acoustic resonator, the method comprising:

forming a resistance layer on an upper surface of a semiconductor substrate, the resistance layer including a recess;

filling the recess with a sacrificial material;

providing a membrane layer on an upper surface of the resistance layer and an upper surface of the sacrificial material;

forming a first electrode on an upper surface of the membrane layer;

forming a piezoelectric layer on the upper surface of the membrane layer and on an upper surface of the first electrode;

forming a second electrode on an upper surface of the piezoelectric layer; and

removing the sacrificial material, thereby forming an air gap between the semiconductor substrate and the membrane layer.

7. (Original) The method as claimed in claim 6, wherein the forming of the resistance layer includes:

depositing a resistance material on the upper surface of the semiconductor substrate;

patterning an air gap forming position on an upper surface of the resistance layer;

removing a portion of the resistance material in the air gap patterning position from the upper surface of the resistance layer to form the recess.

8. (Currently Amended) The method as claimed in claim 7, wherein the patterning ~~pattering~~ of the air gap forming position includes providing a patterning material on an upper surface of the resistance material.

9. (Original) The method as claimed in claim 8, further comprising removing the patterning material after the removing of the portion of the resistance material.

10. (Original) The method as claimed in claim 7, wherein the removing of the portion of the resistance material includes etching the resistance material.

11. (Original) The method as claimed in claim 7, wherein the removing of the portion of the resistance material includes removing all of the resistance material in the air gap portion.

12. (Original) The method as claimed in claim 7, wherein the removing of the portion of the resistance material includes leaving the resistance material at a predetermined thickness in the air gap portion.

13. (Original) The method as claimed in claim 6, further comprising forming a second resistance layer on an upper surface of the recess.

14. (Original) The method as claimed in claim 13, wherein the forming of the second resistance layer includes depositing a second resistance material on upper surfaces of the recess and the resistance layer.

15. (Original) The method as claimed in claim 6, further comprising evening out the upper surface of the resistance layer and the upper surface of the sacrificial material prior to the providing of the membrane layer.

16. (Original) The method as claimed in claim 6, wherein the sacrificial material is polysilicon.

17. (Currently Amended) The method as claimed in claim [[4]] 6, wherein the removing of the sacrificial material includes dry-etching the sacrificial material.

18. (Currently Amended) The method as claimed in claim [[15]] 17, wherein the dry-etching includes using fluorochemical gas in a non-plasma state.

19. (Original) The method as claimed in claim 6, further comprising etching the semiconductor substrate to a predetermined thickness before the forming of the resistance layer.

20. (Original) The method as claimed in claim 6, wherein the forming of the resistance layer includes exposing the semiconductor substrate through the recess.